S/N 09/691,004

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

16 2 3 2067 pp∯icant:

Leonard Forbes et al.

Examiner: Johannes P. Mondt

Sertal No.:

09/691,004

Group Art Unit: 2826

offiled:

October 18, 2000

Docket: 303.324US4

Title:

TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND

METHODS OF FABRICATION AND USE

RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents Washington, D.C. 20231

In response to the Office Action dated 20 May 2002, the applicant requests 28 reconsideration of the above-identified application in view of the following remarks. Claims 36-45, 56-85, and 98-100 are pending in the application, and are rejected. None of the claims have been amended.

Information Disclosure Statement

The applicant filed an Information Disclosure Statement with ten(10) sheets of Form 1449 on 18 October 2000. Copies of the non-patent literature items are attached hereto in response to the Examiner's request. The Examiner is invited to telephone the below-signed attorney if any further copies are needed. The applicant respectfully requests that the references listed on all of the Forms 1449 be considered by the Examiner. Pursuant to the provisions of MPEP 609, the applicant requests that copies of the Forms 1449, initialed as being considered by the Examiner, be returned to the applicant with the next official communication.

Rejection Under 35 U.S.C. § 102

Claim 40 was rejected under 35 USC § 102(e) as being anticipated by Forbes et al. (U.S. Patent No. 5,989,958, Forbes). The applicant respectfully traverses.

The applicant respectfully submits that Forbes is not prior art. Forbes issued on 23 November 1999 from an application filed on 20 August 1998. The above-identified application is a continuation of U.S. Serial No. 08/903,452, filed on 29 July 1997, before the filing date of Forbes.

The applicant respectfully submits that claim 40 is in condition for allowance.